OIPE JC41 OCT 17 2003 PATENT & TRADEMARK OFFICE

PATENT

Case Docket No. IMEC280.001AUS
Date: October 14, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Collaert, et al.
Appl. No.	:	10/621,044
Filed	:	July 15, 2003
For	:	INTEGRATED SEMICONDUCTOR FIN DEVICE AND A METHOD FOR MANUFACTURING SUCH DEVICE
Examiner	:	Unassigned
Group Art Unit	:	2814

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

October 14, 2003
(Date)

Mark M. Abumeri, Reg. No. 43,458

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are:

(X) An Information Disclosure Statement.

(X) A PTO Form 1449 with nine (9) references.

(X) Certified Priority Document for European Patent Application No. 02447135.1, filed July 17, 2002.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

(X) Return prepaid postcard.

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INFORMATION DISCLOSURE STATEMENT

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

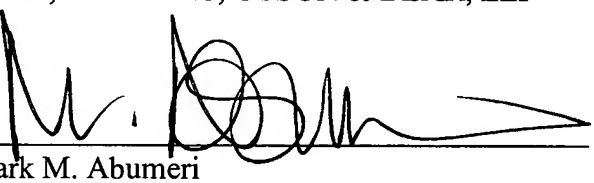
Enclosed is form PTO-1449 listing nine (9) references that are also enclosed.

This Information Disclosure Statement is being filed with an RCE or within three months of the filing date of this application and no fee is required in accordance with 37 C.F.R. § 1.97(b)(1), (b)(2), or (b)(4).

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: October 14, 2003

By: 

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (USE SEVERAL SHEETS IF NECESSARY)	ATTY. DOCKET NO. IMEC280.001AUS	APPLICATION NO. 10/621,044
	APPLICANT Collaert, et al.	
	FILING DATE July 15, 2003	GROUP 2814

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	1	6,118,161	09/12/00	Chapman, et al.			
	2	6,207,511	03/27/01	Chapman, et al.			
	3	6,252,284 B1	06/26/01	Muller, et al.			

*EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	4	Choi, et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era", IEEE Electron Device Letters, vol. 23, no. 1, pp. 25-27, (January 2002).
	5	Choi, et al., "Sub-20nm CMOS FinFET Technologies", IEEE, pp. 421-424, (2001).
	6	Hisamoto, et al., "A Folded-channel MOSFET for Deep-sub-tenth Micron Era", International Electron Devices Meeting, pp. 1032-1034, (1998).
	7	Huang, et al., "Sub-50 nm P-Channel FinFET", IEEE Transactions on Electron Devices, vol. 48, no. 5, pp. 880-886, (May 2001).
	8	Kedzierski, et al., "High-performance symmetric-gate and CMOS-compatible V_t asymmetric-gate FinFET devices", IEEE, pp. 437-440, (2001).
	9	European Search Report dated December 17, 2002 for European Application No. 02 44 7135.1.

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EXAMINER	DATE CONSIDERED

***EXAMINER:** INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.